# CMOS Image Sensors and Interface Circuits

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November 2021 ECE 6422

**Abstract**

*It is an extremely convenient fact that the bandgap of silicon lines up almost exactly with photon energies in the visible range inducing electron hole pairs. This allows the utilization of cheap silicon semiconductors as image sensors, providing designers with unique circuit architecture opportunities at a low cost. This paper seeks to explore the basic principles of operation of silicon based imagers, explain their working principles, and cover current research in the field.*

## I. Introduction

As technology steadily moves along in accordance to Moore's law engineers ability to place complex systems in even smaller, lower power, and remote locations also increases. An area this can be readily seen is image sensors. The current iPhone contains a 12 megapixel camera with a pixel size of 1.8 microns. Twenty years ago this was a professional photographer's level of equipment, now everyone has it in their pocket. The enabling technology behind these advances is the progress of silicon transistor technology, allowing for cost effective but technologically impressive advances in countless areas.

## II. Working Principles

A basic silicon CMOS (Complementary Metal Oxide Semiconductor) image sensor is made of an array of photodiodes. Each photodiode converts photons to current and some amplification or readout circuitry coverts this value to a digital pixel intensity [1]. Typically the charge is integrated via some capacitance over some capture time to increase accuracy. Each photodiode in the array serves as one pixel. In charge coupled devices (CCD) each pixel charge is transported to an output capacitor to obtain a voltage, which is then buffered and read out serially. CMOS image sensors have largely replaced CCD image sensors in recent years, so they will not be covered here.

The push to move image sensors to a CMOS system instead of a CCD system arises from the benefit of CMOS integration. With deep submicron technologies CMOS devices are now small enough to incorporate both analog and digital interface circuits right next to each pixel in the array. This allows a large degree of control over readout characteristics such as tim-

ing, amplification, etc. It is important to note however that pixel sizes are still typically on the order of microns (though this is an active field of research). This is to due to the fact that noise characteristics increase and sensitivity decreases with decreasing pixel size, making it difficult to construct robust, accurate sensors with very small pixel sizes (<1 um). While smaller pixels capture less light (decreasing dynamic range), they also offer a higher resolution, and techniques such as pixel binning solve the low light drawback.

A typical image acquisition process consists of focusing photons on the sensor, transducing the optical signal to an electrical current, integrating the electrical current to create a voltage over time, converting the voltage to a digital value, then carrying out image post processing. This process can be seen visually in Figure 2.

The working principle of any electronic imager is the photoelectric effect, simply saying that when a photon of some energy greater than the bandgap of the semiconductor strikes a semiconductor material, an electron will be knocked into the conduction band, generating a photocurrent. Photodiodes are typically simply reverse biased PN junctions (though pinned diode structures are commonly used) with some junction capacitance created by the depletion region. This junction capacitance is typically used as the previously mentioned integration capacitance. The equation

$$Q = CV \tag{1}$$

obviously governs the capacitor, so the quantity $\frac{Volts}{Electron}$ present on the capacitor is the important quantity called the conversion gain of the pixel, typically on the order of uv/electron. This leads conveniently into the next important quantity of the photodiode, the quantum efficiency. Defined as a function of wavelength $\lambda$ the quantum efficiency is the fraction of incident photons at some wavelength that contribute to the photocurrent, see Figure 1 for an example QE curve for a visible range imager.

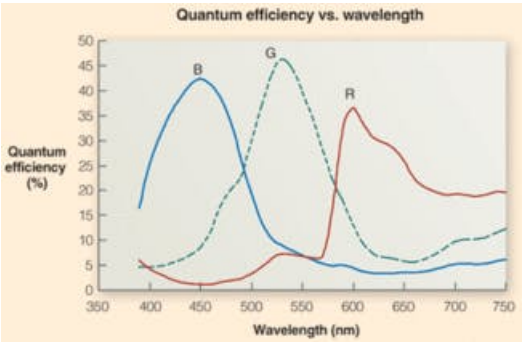


Figure 1: Quantum Efficiency of CMOS Imager

The higher the QE at a given wavelength the more effective the photodiode is at that wavelength. The other remaining important parameter of the photodiode is the dark current, or the current when no light is applied. This is due to non idealities (noise, unwanted resistance, etc) and generally has a negative effect by lowering the dynamic range of the pixel.

Mechanisms that cause dark current can be things such as flicker noise, shot noise, or non zero off current (current flowing through reset transistor). Generally dark current is higher in CMOS imagers than CCD systems, due to the active components in CMOS systems. CMOS imagers do have the advantage however of utilizing analog noise reduction techniques such as CDS or sampling techniques. They can also take advantage of digital calibration techniques at the pixel level. Overall the system noise can generally be determined solely by considering shot noise, flicker noise, readout quantization

noise, and the variation in dark current (since DC dark current can be removed by both DC decoupling and in software). [1]

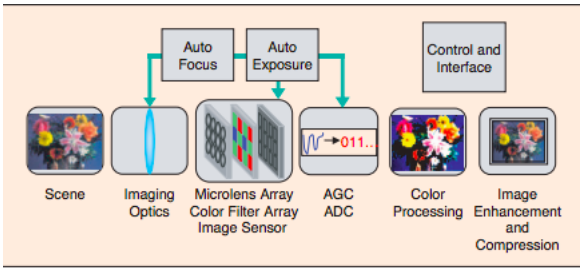


Figure 2: Typical Image Pipeline

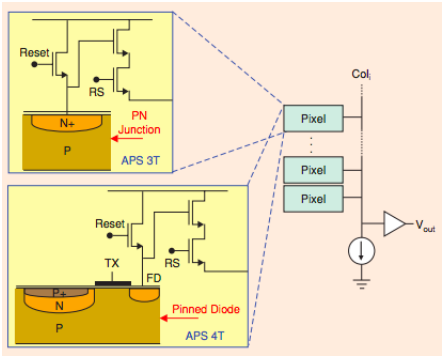


Figure 3: 3T and 4T Readout Circuits

## III. Interface and Pixel Readout

### i. Pixel Readout Circuits

There are various architectures available for pixel readout circuits. The simplest is simply 1 select transistor per pixel, which was quickly done away with for a 3 transistor architecture (Figure 3) which consists of a reset transistor, a select transistor, and a source follower transistor to drive current to readout circuits (data converters). While this is a viable way of doing things, it lacks a method to multiplex the photodiode itself, reducing control over photodiode charge (possibly not allowing full charge depletion). The most common circuit currently is the 4T readout circuit (Figure 3), and its variant, the 1.75T readout circuit (Figure 4). The 4T readout circuit consists of the same elements as the 3T readout circuit, but adds a pinned photodiode, adding a p+ doped layer on top of the n type layer, forming a buried photodiode. This allows for full charge depletion due to both the p+ cap region and p type substrate allowing for charge diffusion, and almost completely removing KTC noise by greatly reducing the charge present on the readout capacitor, while increasing its voltage due to the lowered capacitance. This greatly improves pixel quality by reducing noise and increasing readout speed (by increasing readout current and reducing readout capacitance). The contribution of this pinned photodiode to the field of imagers in general can not be overstated. The pinned photodiode is activated by the 4th gate in the circuit, hence the colloquial 4T. A timing diagram of the 4T readout circuit can be seen in Figure 6.

Initially the circuit is reset and some integration time is allowed for charge to be built up on the interface capacitance of the diode. The pinned photodiode gate is then set high, creating the traditional MOS channel. The signal drives the gate of the source follower circuit, which drives current into the capacitive load of the data converter. This readout process remains basically the same for the 3T and 1.75T circuits, with the 3T circuit losing the ability to multiplex with the $X_i$ signal.

The 1.75T readout circuit simply takes the 4T readout circuit and shares the source follower

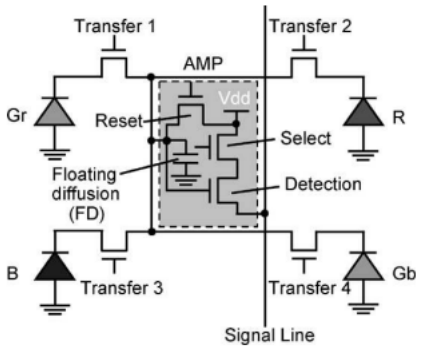


Figure 4: 1.75T Readout Circuit

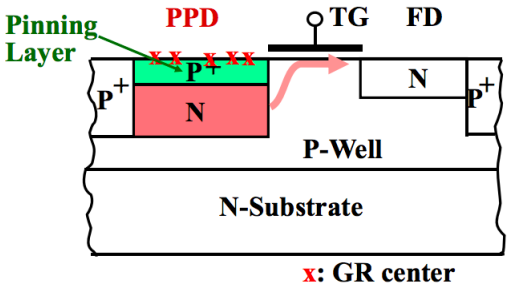


Figure 5: Pinned Photodiode

among multiple pixels, and multiplexes with the pinned diode enable signal. [1]

## ii. Data Converter Circuits

The next big component of the readout circuitry is the ADC (Analog to Digital Converter). Typically each column of the image sensor gets its own ADC, allowing full parallel operation, and quick readout. While any ADC architecture may be used, the most common is the single slope ADC, which operates by digitally sloping one input to a comparator, while the buffered pixel value is the other input to

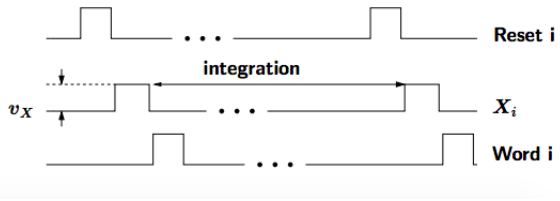


Figure 6: Timing Diagram of 4T Circuit

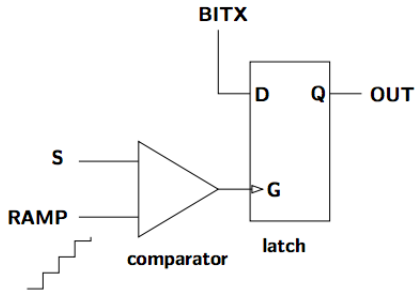


Figure 7: Single Slope ADC Architecture

the comparator. The architecture can be seen in Figure 8. When the output changes state the value is recorded in a latch. This is a space and power efficient ADC, requiring only a digital counter, comparator, and latch [6].

It is also possible to place one ADC per pixel, or small group of pixels, obviously decreasing readout time at the expense of power and area. Typical ADC's used are in the range of 10 bit resolution with mW level power draw (reference needed here). Though the single slope ADC is the most common architecture used in the readout circuit, work has been carried out utilizing other architectures, such as the a successive approximation register (SAR) ADC, or a delta-sigma ADC, and even noise shaping SAR ADC's, combining the delta sigma

approach with a SAR [10]. The single slope ADC has an exponentially scaling bit width vs. power relationship and bit width vs. conversion time relationship caused by the single step counter requiring exponentially more steps for each conversion, drawing large amounts of dynamic power for higher light intensity levels [1].

The SAR ADC avoids this problem due to its binary search nature, but has a very large area requirement driven entirely by capacitive digital to analog converter (DAC) bank. While resistive DAC's are available they have poor linearity and much higher static power consumption [11]. The large area requirement stems from the fact that one must have exponentially sized capacitances, which consume exponential area. For example with a unit capacitance $C_{unit}$ of 20fF, a 10 bit DAC must have a max capacitance of 512*$C_{unit}$ (around 1pF), which can take up to a few square millimeters of chip area depending on technology [2]. For image sensors this implies one can not have a single ADC for each pixel, or generally even each column. While this is disadvantageous, there are positives such are higher noise rejection in oversampling architectures or lower static and dynamic power draw [2].

Oversampling architectures in particular are an exciting area of research [9]. While the basic idea combines the SAR and Delta Sigma architectures the implementation details are quite dense. See figure 8 for an example system. The initial voltage is read in and added to some fed back and inverted version of a previous DAC output. The voltage $V_{res}$ contains information about both the difference in DAC out and input voltage, as well as the input referred noise of the comparator. The system allows one to remove these noises at low frequencies, similar to the traditional delta sigma approach. This approach allows the designer to remove lower frequency noise such as flicker noise, as well as quantization noise from the system, increasing all aspects of the Signal to Noise Ratio (SNR). This approach also allows for a smaller capacitor bank (an 8 bit CDAC in an NS-SAR has been shown to obtain 10 bit resolutions), potentially allowing more data converters to be placed on die with the pixel array, removing the main drawback of the SAR.

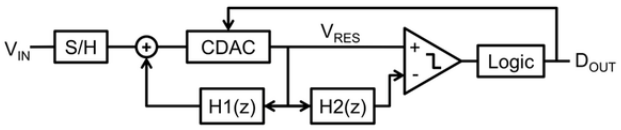


Figure 8: Noise Shaping SAR

## IV. Conclusion

The current direction of research in the electronics of CMOS imagers is primarily towards the data converter. The ability to control shape the noise spectrum in SAR data converters leads to exciting opportunities to deal with non idealities in both the analog readout components as well as the photodiode itself. Research is also being carried out in noise reduction of the PD cells themselves. The state of the art is steadily progressing towards sub-micron pixel size, with low milliwatt level power draws of the sensing array.

## References

[1] . El Gamal and H. Eltoukhy, "CMOS image sensors," in IEEE Circuits

and Devices Magazine, vol. 21, no. 3, pp. 6-20, May-June 2005, doi: 10.1109/MCD.2005.1438751.

[2] . D. Choo et al., "5.2 Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), 2019, pp. 96-98, doi: 10.1109/ISSCC.2019.8662306.

[3] . Kumagai et al., "A 1/4-inch 3.9Mpixel low-power event-driven back-illuminated stacked CMOS image sensor," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), 2018, pp. 86-88, doi: 10.1109/ISSCC.2018.8310196.

[4] bbas, Class Lecture, Topic: "CMOS image sensors", EE 392, Stanford University, Stanford

[5] . Teranishi, "The Pinned Photodiode", CERN, June 2nd 2016

[6] . Jeon, S. Hong and O. Kwon, "A low-power 10-bit single-slope ADC using power gating and multi-clocks for CMOS image sensors," 2016 International SoC Design Conference (ISOCC), 2016, pp. 257-258, doi: 10.1109/ISOCC.2016.7799775.

[7] . Hwang et al., "A 2.7-M Pixels 64-mW CMOS Image Sensor With Multicolumn-Parallel Noise-Shaping SAR ADCs," in IEEE Transactions on Electron Devices, vol. 65, no. 3, pp. 1119-1126, March 2018, doi: 10.1109/TED.2018.2795005.

[8] . R. Fossum and D. B. Hondongwa, "A Review of the Pinned Photodiode for CCD and CMOS Image Sensors," in IEEE Journal of the Electron Devices Society, vol. 2, no. 3, pp. 33-43, May 2014, doi: 10.1109/JEDS.2014.2306412.

[9] .A Fredenburg, "NOISE-SHAPING SAR ADCS", Ph.D Dissertation, School of Electrical and Computer Engineering, Universtiy of Michigan, Ann Arbor, MI, 2015

[10] ouveia, L.C.P. and Choubey, B. (2016), "Advances on CMOS image sensors", Sensor Review, Vol. 36 No. 3, pp. 231-239.

[11] . Boina and R. Paily, "Comparison of DAC architectures of sar ADCS," Fourth International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom2012), 2012, pp. 38-43, doi: 10.1049/cp.2012.2490.